AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A context switching unit for switching a plurality of contexts, the context switching unit comprising:

a register file having stored a context related to a thread to be executed by an arithmetic logic unit or a memory access unit, the register file comprising a register read port, a register write port, a context-switching read port, and a context-switching write port;

a context cache used exclusively for ~~caching a context,~~ saving and restoring contexts, the context cache comprising a read port and a write port, being connected directly to the register ~~file, and being contained~~ file and integrated in a central processing unit ~~in a on-chip manner;~~ on a chip, the context cache being not connected to a memory through a bus, which connects the memory, an instruction cache and a data cache to each other, and being independent from a memory system including the memory, the instruction cache and the data cache, to realize context switching at a high processing speed without interference from the bus;

a context switching bus for connecting the register file and the context cache, the context switching bus comprising a restore bus and a save bus for connecting the read port and the write port of the context cache to the context-switching write port and the context-switching read port of the register file respectively; and

a thread control unit for controlling data transfer between the context cache and the register file, the thread control unit comprising a thread identifier table for storing a thread identifier for identifying the context of a thread stored in the context cache and being connected in parallel with the arithmetic logic unit and the memory access unit,

~~wherein~~ wherein, in case of a context switch operation which executes both a save operation for saving a context from the register file to the context cache and a restore operation for restoring a context from the context cache to the register file in parallel at the same time, the thread control unit receives a context switch instruction for executing ~~a save operation~~ the context switch operation with ~~and a restore operation concurrently and~~ the identifier of a new thread to be ~~interchanged, when a context switch which executes both a context save operation and a context restore operation in parallel occurs;~~interchanged;

the thread control unit obtains a restore address where a new context to be interchanged is stored in the context cache and ~~the save~~ a save register identifier indicating ~~the location~~ a location where ~~the current~~ a current context is stored in the register file, by searching through the thread identifier table in accordance with the thread identifier;

the thread control unit sends the obtained address to the context cache and ~~sends~~ the register identifier to the register file ~~concurrently;~~

in parallel at the same time;

the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port to the save bus for the save operation and holds ~~and, concurrently writes~~ the data of the context to be ~~restored,~~ in parallel at the same time, sent from the read port of the context cache to the context-switching write port through the restore ~~bus, in the register corresponding to the register identifier;~~ for the restore operation;

the context cache, in accordance with the address given by the thread control unit, outputs the data of ~~the context~~ a context to be restored from the read port to the restore bus for the restore operation and holds ~~and, concurrently writes~~ the data of the context to be saved in parallel at the same time, sent from the context-switching read port of the register file to the write port via the save ~~bus;~~ bus for the save operation; and

whereby the context switching unit switches contexts ~~by executing an operation~~

~~for restoring a context from~~ the context ~~cache to the register file and an operation for saving a context from the register file to the context cache concurrently.~~ switch operation which executes both the restore operation and the save operation in parallel at the same time.

2. (Currently Amended) The context switching unit according to Claim 1, wherein the context switching bus has a bus width greater than ~~the bit~~ a bit width of the register file.

3. (Previously Presented) The context switching unit according to Claim 1, wherein the thread control unit comprises as many thread identifier tables as required to identify contexts cached in the context cache.

4. (Canceled)

5. (Currently Amended) The context switching unit according to Claim 1, wherein the thread control unit saves the context of the current thread from the register file to the context cache and sends the context of a new thread from the context cache to the register file ~~concurrently~~ in parallel at the same time to automatically interchange a required number of data items between the register file and the context cache, when software, such as an operating system, issues a swap instruction for interchanging contexts, including a thread identifier as an operand, if the swap instruction is executed.

6. (Previously Presented) The context switching unit according to Claim 1, wherein the thread control unit transfers the data of a context from the register file to the context cache and does not transfer the data of a context from the context cache to the register file, when software, such as an operating system, issues a backup instruction for saving a context, including a thread identifier as an operand, if the backup instruction

is executed.

7. (Previously Presented) The context switching unit according to Claim 1, wherein the thread control unit transfers the data of a context from the context cache to the register file and does not transfer the data of a context from the register file to the context cache, when software, such as an operating system, issues a restore instruction for restoring a context, including a thread identifier as an operand, if the restore instruction is executed.

8. (Currently Amended) A central processing unit comprising:

a context switching unit according to ~~Claim1;~~ Claim 1;

~~an instruction~~ the instruction cache for caching an instruction and ~~a data~~ the data cache for caching data;

an instruction fetch unit for fetching ~~an instruction~~ the instruction from the instruction cache and decoding the instruction;

~~an arithmetic logic unit for performing an operation in accordance with an instruction stored in the register file and writing the result of the operation back in the register file;~~

~~a memory~~ the memory access unit for ~~receiving an operand and an instruction from the register file,~~ accessing the data ~~cache,~~ cache and memory, and executing a load or store operation; and

an arithmetic bus for connecting the register file, the arithmetic logic unit, the memory access unit, and the thread control unit in parallel.

9. (Previously Presented) The central processing unit according to Claim 8, wherein the memory access unit sends an address and data to the data cache and

stores the data in the data cache when a store instruction is given, and the memory access unit sends an address to the data cache, reads data from the data cache, and writes the read data back into the register file when a load instruction is given.

10. (Currently Amended) A context switching method for switching a plurality of contexts by using a context switching unit comprising:

storing a context related to a thread in a register file to be executed by an arithmetic logic unit or a memory access unit, the register file comprising a register read port, a register write port, a context-switching read port, and a context-switching write port;

saving and restoring contexts exclusively ~~caching a context,~~ in a context ~~cache~~ cache, the context cache comprising a read port and a write port, being connected directly to the register ~~file, and being contained~~ file and integrated in a central processing unit ~~in a on-chip manner;~~ on a chip, the context cache being not connected to a memory through a bus, which connects the memory, an instruction cache and a data cache to each other, and being independent from a memory system including the memory, the instruction cache and the data cache, to realize context switching at a high processing speed without interference from the bus;

connecting the register file and the context cache with a context switching bus, the context switching bus comprising a restore bus and a save bus for connecting the read port and the write port of the context cache to the context-switching write port and the context-switching read port of the register file respectively; and

controlling data transfer between the context cache and the register file using a thread control unit, the thread control unit comprising a thread identifier table for storing a thread identifier for identifying the context of a thread stored in the context cache and being connected in parallel with the arithmetic logic unit and the memory access unit,

~~wherein~~ wherein, in case of a context switch operation which executes both a save operation for saving a context from the register file to the context cache and a

restore operation for restoring a context from the context cache to the register file in parallel at the same time, the thread control unit receives a context switch instruction for executing ~~a save operation and a restore~~ the context switch operation ~~concurrently and~~ with the identifier of a new thread to be ~~interchanged, when a context switch which executes both a context save operation and a context restore operation in parallel occurs;~~interchanged;

the thread control unit obtains a restore address where a new context to be interchanged is stored in the context cache and ~~the save~~ a save register identifier indicating ~~the location~~ a location where ~~the current~~ a current context is stored in the register file, by searching through the thread identifier table in accordance with the thread identifier;

the thread control unit sends the obtained address to the context cache and ~~sends~~ the register identifier to the register file ~~concurrently;~~in parallel at the same time;

the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port ~~and, concurrently writes~~ to the save bus for the save operation and holds the data of the context to be ~~restored,~~ restored in parallel at the same time, sent from the read port of the context cache to the context-switching write port through the restore ~~bus, in the register corresponding to the register identifier;~~ bus for the restore operation;

the context cache, in accordance with the address given by the thread control unit, outputs the data of the context to be restored from the read port ~~and, concurrently writes~~ to the restore bus for the restore operation and holds the data of the context to be saved in parallel at the same time, sent from the context-switching read port of the register file to the write port via the save ~~bus;~~ bus; for the save operation; and

whereby the context switching unit switches contexts by ~~executing an operation for restoring a context from~~ the context switch operation which executes both the restore ~~cache to the register file and an operation for saving a context from the register file to the context cache concurrently.~~operation and the save operation in parallel at the

same time.

11. (Previously Presented) The context switching method according to Claim 10, saving the context of the current thread from the register file to the context cache and sending the context of a new thread from the context cache to the register file concurrently to automatically interchange a required number of data items between the register file and the context cache, when software, such as an operating system, issuing a swap instruction for interchanging contexts, including a thread identifier as an operand, if the swap instruction is executed.

12. (Previously Presented) The context switching method according to Claim 10, transferring the data of a context from the register file to the context cache and not transferring the data of a context from the context cache to the register file, when software, such as an operating system, issuing a backup instruction for saving a context, including a thread identifier as an operand, if the backup instruction is executed.

13. (Previously Presented) The context switching method according to Claim 10, transferring the data of a context from the context cache to the register file and not transferring the data of a context from the register file to the context cache, when software, such as an operating system, issuing a restore instruction for restoring a context, including a thread identifier as an operand, if the restore instruction is executed.

14. (Currently Amended) A computer comprising a context switching program for switching a plurality of contexts ~~on a computer~~ by using a context switching unit the context switching unit comprising:

a register file having stored a context related to a thread to be executed by an

arithmetic logic unit or a memory access unit, the register file comprising a register read port, a register write port, a context-switching read port, and a context-switching write port;

a context cache used exclusively for ~~caching a context,~~ saving and restoring contexts, the context cache comprising a read port and a write port, ~~being~~ connected directly to the register ~~file, and being contained~~ file and integrated in a central processing unit ~~in a on-chip manner;~~ on a chip, the context cache being not connected to a memory through a bus, which connects the memory, an instruction cache and a data cache to each other, and being independent from a memory system including the memory, the instruction cache and the data cache, to realize context switching at a high processing speed without interference from the bus;

a context switching bus for connecting the register file and the context cache, the context switching bus comprising a restore bus and a save bus for connecting the read port and the write port of the context cache to the context-switching write port and the context-switching read port of the register file respectively; and

a thread control unit for controlling data transfer between the context cache and the register file, the thread control unit comprising a thread identifier table for storing a thread identifier for identifying the context of a thread stored in the context cache and being connected in parallel with the arithmetic logic unit and the memory access unit,

the context switching program ~~permits~~ causing the computer to execute:

a step ~~in which~~ wherein, in case of a context switch operation which executes both a save operation for saving a context from the register file to the context cache and a restore operation for restoring a context from the context cache to the register file in parallel at the same time, the thread control unit receives a context switch instruction for executing ~~a save operation and a restore~~ the context switch operation ~~concurrently and~~ with the identifier of a new thread to be ~~interchanged, when a context switch which executes both a context save operation and a context restore operation in parallel occurs;~~ interchanged;

a step in which the thread control unit obtains a restore address where a new context to be interchanged is stored in the context cache and the save register identifier indicating the location where the current context is stored in the register file, by searching through the thread identifier table in accordance with the thread identifier;

a step in which the thread control unit sends the obtained address to the context cache and ~~sends~~ the register identifier to the register file ~~concurrently;~~ in parallel at the same time;

a step in which the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port to the save bus for the save operation and holds ~~and, concurrently writes~~ the data of the context to be ~~restored,~~ restored in parallel at the same time, sent from the read port of the context cache to the context-switching write port through the restore ~~bus, in the register corresponding to the register identifier;~~ bus for the restore operation in the register corresponding to the register identifier;

a step in which the context cache, in accordance with the address given by the thread control unit, outputs the data of the context to be restored from the read port ~~and, concurrently writes~~ to the restore bus for the restore operation and holds the data of the context to be saved in parallel at the same time, sent from the context-switching read port of the register file to the write port via the save ~~bus;~~ bus for the save operation; and

~~wherein~~ whereby the context switching unit switches contexts by ~~executing an operation for restoring a context from~~ the context ~~cache to the register file and an~~ switch operation which executes both the restore operation ~~for saving a context from the register file to the context cache concurrently.~~ and the save operation in parallel at the same time.

15. (Cancelled)